REMARKS

Reconsideration of this application, as presently amended, is respectfully requested. Claims 1-8 are pending in this application. Claims 1 and 7-8 stand rejected. Claims 2-6 were objected to as being dependent upon a rejected base claim but were indicated to be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

Claim Rejections-35 U.S.C. §103

Claims 1 and 7 were rejected under 35 U.S.C. §103(a) as being unpatentable over **Utsugi** (JP-2-67665) in view of **Maas et al.** (USP 6,763,036). Claims 1 and 8 were rejected under 35 U.S.C. §103(a) as being unpatentable over Applicants' acknowledged prior art (**AAPA**) in view of **Utsugi** and **Maas et al.** These rejections, to the extent they are considered to apply to the amended claims, are respectfully traversed.

Claim 1 has been amended to clarify that the "input data sequence" held by the first parallel shift register is a sequence of data elements each having a first data width. The language defining the "second parallel shift register" has also been amended in a manner similar to the "first parallel shift register."

Utsugi discloses an interface circuit that is capable of providing an interface for both 8-bit data and 16-bit data using registers that are only 8-bit registers. More specifically, as discussed in the English translation of the Japanese Office Action dated October 17, 2005 (see page 2 of Japanese Office Action), each of the registers 31-33 are 8-bit registers. As indicated in

the English language Abstract of **Utsugi**, when processing data of 16-bit width, 8-bit input data are successively stored in the register 31. Apparently, the most significant 8-bits (higher rank) of the 16-bit data are transferred to the register 32. The next 8-bits are transferred to the register 33. Thus, when processing data having 16-bit width, the first 8-bits are apparently held in register 32 until the next 8-bits are transferred to register 33. When processing 8-bit data, it is apparently unnecessary to hold the preceding 8-bits in a register because only 8-bits are being processed.

Thus, **Utsugi** teaches an interface that can handle both 8-bit data and 16-bit data using only 8-bit registers. Presumably, an advantage of using only 8-bit registers, as opposed to 16-bit registers, is that 8-bit registers are cheaper.

As set forth on page 2, Item 3 of the Office Action, the Examiner considers the 8-bit data and 16-bit data that can be processed by the interface circuitry 31-33 to be "any one of a plurality of input data sequences having different data widths." Further, the Examiner considers the register 31 to correspond to the "first parallel shift register for holding said input data sequence" and considers the registers 32, 33 to correspond to the "second parallel shift register ....for outputting said input data as a data sequence having said prescribed data width."

Further, as noted on page 2 of the English translation of the Japanese Office Action, it appears that **Utsugi** includes is some sort of switch circuit to selectively transfer data from the register 31 to either the register 32 or 33.

The Examiner asserts that **Utsugi** does not disclose the claimed switch matrix, and applies **Maas et al.** to teach a switch matrix.

However, it is respectfully submitted that the neither **Utsugi** nor **Maas et al.**, whether taken alone or in combination, disclose or suggest the elements currently recited in amended claim 1. More specifically, neither **Utsugi** nor **Maas et al.** disclose or suggest "a first parallel shift register that receives parallel input data having a first data width, wherein the first parallel shift register receives a sequence of data elements respectively having the first data width and holds the sequence of data elements together in the first parallel shift register," as recited in claim 1.

In contrast to the invention recited in amended claim 1, the register 31 of **Utsugi** receives in parallel 8-bit data and holds the 8-bit data. *However, the register 31 of* ***Utsugi*** *does not receive and hold (i.e., store) a sequence of data elements (each having 8-bit length) together in the register 31.* Instead, the register 31 of **Utsugi** successively stores the 8-bit data, one data element at a time.

Further, neither **Utsugi** nor **Maas et al.** disclose or suggest "a second parallel shift register receiving the data output from said switch matrix as input data, and outputting said input data as parallel output data having a second data width different from the first data width, wherein the second parallel shift register outputs said input data as a sequence of data elements respectively having the second data width," as presently recited in claim 1.

As noted above, according to **Utsugi**, when processing data of 16-bit width, 8-bit input data are successively stored in the register 31. Apparently, the most significant 8-bits (higher rank) of the 16-bit data are transferred to the register 32. The next 8-bits are transferred to the register 33. Thus, when processing data having 16-bit width, the first 8-bits are apparently held

in register 32 until the next 8-bits are transferred to register 33. However, unlike the presently claimed invention, the registers 32, 33 of **Utsugi** do not output the input data *as a sequence of data elements respectively having the second data width.*

Moreover, as noted above, the Examiner finds that **Utsugi** does not teach the claimed switch matrix and relies on the **Maas et al.** reference to teach the claimed switch matrix. However, it is submitted that **Maas et al.** do not alleviate any of the deficiencies of **Utsugi** discussed above.

Specifically, **Maas et al.** do not disclose or suggest "a first parallel shift register that receives parallel input data having a first data width, wherein the first parallel shift register receives a sequence of data elements respectively having the first data width and holds the sequence of data elements together in the first parallel shift register." Similarly, **Maas et al.** do not disclose or suggest the "second parallel shift register."

Therefore, it is submitted that the combination of **Utsugi** and **Maas et al.** does not result in the claimed invention. Accordingly, reconsideration and withdrawal of the rejection of claims 1 and 7 under §103 over **Utsugi** in view of **Maas et al.** are respectfully requested.

Rejection of claims 1 and 8 under 35 U.S.C. §103(a) as being unpatentable over Applicants' acknowledged prior art (AAPA) in view of Utsugi and Maas et al.

Initially, clarification is requested regarding the rejection of claim 1 over **AAPA** in view of **Utsugi** and **Maas et al.** Specifically, claim 1 was rejected above over ***only*** **Utsugi** and **Maas et al.** Therefore, it would appear that the Examiner is admitting that the combination of **Utsugi**

and **Maas et al.** does ***not*** disclose all the features of claim 1, and it was therefore necessary to further combine **AAPA** with the **Utsugi** and **Maas et al.** references to reject claim 1.

Alternatively, it may be that the Examiner intended to reject only claim 8 over the combination of **AAPA** in view of **Utsugi** and **Maas et al.** Clarification is respectfully requested.

In any event, it is submitted that **AAPA** does not alleviate any of the deficiencies of **Utsugi** and **Maas et al.** discussed above.

Specifically, on page 4, lines 6-9 of the Office Action, the Examiner cites **AAPA** to teach a data sequence conversion circuit between a jaggy correction circuit and a line printhead, and admits that AAPA does not include any of the features recited in claim 1 (i.e., first parallel shift register, switch matrix, second parallel shift register).

Therefore, it is submitted that **AAPA** do not alleviate any of the deficiencies of **Utsugi** and **Maas et al.** discussed above with respect to the rejection of claim 1. Claim 8 is therefore allowable by virtue of its dependency on claim 1.

CONCLUSION

In view of the foregoing amendments and accompanying remarks, it is submitted that all pending claims are in condition for allowance. A prompt and favorable reconsideration of the rejection and an indication of allowability of all pending claims are earnestly solicited.

If the Examiner believes that there are issues remaining to be resolved in this application, the Examiner is invited to contact the undersigned attorney at the telephone number indicated below to arrange for an interview to expedite and complete prosecution of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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